IN THE SPECIFICATION

Please amend the Specification as follows:

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FIG. 2b shows the structure of these N time-multiplexed allpass filters of order N with a sampling rate of f.sub.s'=f.sub.s/N which is only different to the allpass filter first order shown in FIG. 2a in that the delay elements now have ~~order N~~ delay NT and the sampling rate is decreased, since the sampling rate decimation by N at the output of the polyphase filter is shifted to the input of the branch filter.

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Therefore, the polyphase filter according to the first preferred embodiment of the present invention comprises: a first delay element 1 with a delay ~~N~~ NT that receives the input signal t(k); a first adder 3 that receives the output signal of said first delay element 1 at a first input for the first summand; a second delay element 2 with a delay ~~N~~ NT that receives the sum produced by said first adder 3; a first subtracter 4 that receives the input signal t(k) at a first input for the minuend and the output signal of the second delay element 2 at a second input for the subtrahend; and a first multiplier 5 that receives the calculated difference of the first subtracter 4, multiplies it respectively with a predetermined multiplication coefficient .alpha.(k) and outputs the calculated product to a second input of the first adder 3 that receives the second summand, wherein in the sum produced by said first adder 3 builds the output signal u(k) of the filter.

On pages 8-9:

According to the second preferred embodiment of the present invention the polyphase filter with branch filters of order 2.N additionally respectively comprises N time-multiplex coefficients .alpha..sub.r and .chi..sub.r with r=0, 1, . . . N-1 instead of the coefficients .alpha. and .chi. shown in FIG. 4. Therefore, the polyphase filter according to the second embodiment of the present invention as shown in FIG. 3 comprises additionally to all components shown in FIG. 1: a second adder 6 that receives the output signal of the second delay element 2 at a first input for the first summand; a third delay element 7 with a delay ~~N~~ NT that receives the sum produced by said second adder 6; a second subtracter 8 that receives the sum produced by said first adder 3 at a first input for the minuend and the output signal of the third delay element 7 at a second input for the subtrahend; and a second multiplier 9 that receives the calculated difference of the second subtracter 8, multiplies it respectively with a predetermined multiplication coefficient .chi.(k) and outputs the calculated product to a second input of the second adder 6 that receives the second summand, wherein the sum produced by said second adder 6 builds the output signal u(k) of the branch filters.